WHAT IS CLAIMED IS:

1. A method of safely shutting down an embedded system based computer under an OS (operating system), the computer including a power switch controlled by an input/output (I/O) control chip, the power switch having a power button, the power button being adapted to press for causing the I/O control chip to trigger a system chipset so that a CPU (central processing unit) performs the steps of:

(a) causing the triggered system chip to issue an interrupt request (IRQ) to the CPU and receiving the same responsive to triggering the system chipset by the I/O control chip;

(b) activating a service routine of the OS for determining whether the IRQ is issued by the pressed power button; and

(c) terminating all running processes of the OS and performing a soft-off for stopping supplying power from a power supply to the computer if the determination in the step (b) is positive.

2. The method of claim 1, further comprising the step (d) of waiting the system chip to issue an IRQ if the determination in the step (b) is negative.

3. The method of claim 1, wherein responsive to pressing the power button the CPU runs the service routine and performs the steps of:

(e) determining whether the power button is pressed or not;

(f) terminating all processes being run by the OS if the determination in the step (e) is positive;

(g) writing a set value into a soft-off register of the I/O control chip; and

(h) causing the power switch to stop supplying power from the power supply to the computer responsive to writing the set value into the soft-off register and disabling the same.

4. The method of claim 3, further comprising the step (i) of continuously determining whether the power button is pressed or not if the determination in

the step (e) is negative.

5. The method of claim 1, wherein the system chipset is a south bridge.